**Amendments to th Claims**

1-8 (Cancelled)

9. (Currently amended): A method of forming a floating gate transistor comprising:

forming an oxide-containing layer over a semiconductive substrate;

forming a first layer of homogeneously conductively doped semiconductive material ~~over a semiconductive substrate~~ upon the oxide-containing layer, wherein the first layer of conductively doped semiconductive material contacts the oxide layer;

forming a second layer of substantially undoped semiconductive material over the first layer;

forming a third layer comprising dielectric material over the second layer;

forming a fourth layer comprising conductive material over the third layer; and

forming a floating gate transistor comprising the first, second, third, and fourth layers.

10. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy at least 25 percent of the floating gate thickness.

11. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness.

12. The method of claim 9, wherein the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

13. (Currently amended): The method of claim 9, wherein the forming of the first layer comprises:

forming a layer ~~of~~ comprising polysilicon ~~over the substrate~~ upon the oxide layer; and

doping the polysilicon layer with phosphorous dopant material to a concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

14. The method of claim 9, wherein:

the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness; and

the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

25. (Currently amended): A method of forming a floating gate transistor comprising:

forming a first oxide-containing layer over a substrate;

forming a first layer ~~of~~ comprising polysilicon ~~over a substrate~~ upon the first oxide-containing layer to a first thickness, the first layer comprising polysilicon being in contact with the first oxide-containing layer;

however,
doping the first layer ~~of~~ comprising polysilicon to a degree sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.;

after the doping, forming a second layer ~~of~~ comprising polysilicon over the first layer ~~of~~ comprising polysilicon to a second thickness;

oxidizing the substrate to form a ~~first~~ second oxide-containing layer over the second layer ~~of~~ comprising polysilicon;

forming a layer ~~of~~ comprising nitride over the ~~first~~ second oxide-containing layer;

oxidizing the substrate to form a ~~second~~ third oxide-containing layer over the layer ~~of~~ comprising nitride;

forming a third layer ~~of~~ comprising polysilicon over the ~~second~~ third oxide-containing layer; and

etching at least some of the layers to provide a floating gate transistor over the substrate.

26. The method of claim 25, wherein the first and second thicknesses are substantially the same.

27. The method of claim 25, wherein the first and second thicknesses are different.

28. The method of claim 25, wherein the first and second thicknesses comprise an aggregate thickness and the first thickness constitutes less than or equal to about 75 percent of the aggregate thickness.

29. The method of claim 25, wherein the first thickness is less than about 550 Angstroms.

30. The method of claim 25, wherein the first thickness is between 450 Angstroms and 550 Angstroms.

31. (Currently amended): The method of claim 25, wherein the forming of the second layer ~~of~~ comprising polysilicon comprises forming the layer to have a sheet resistance which is greater than the sheet resistance of the first layer ~~of~~ comprising polysilicon.

41-71 (Cancelled).

72. (New): A method for enhancing data retention of a floating gate transistor comprising:

forming an oxide-containing layer over a substrate; and

forming a silicon-containing material upon the oxide-containing layer, the silicon-containing material having a thickness, the silicon-containing material having a first region in direct physical contact with the oxide-containing layer and a second region spaced form the oxide-containing layer by the first region; the first region having a higher homogeneous concentration of conductivity enhancing impurity than any conductivity enhancing impurity in the second region.

73. (New): The method of claim 72, wherein the silicon-containing material comprises polysilicon.

74. (New): The method of claim 72, wherein the first region has a thickness of at least 25 percent of the thickness of silicon-containing material.

75. (New): The method of claim 72, wherein the first region has a thickness of about 25 to 75 percent of the thickness of silicon-containing material.

76. (New): The method of claim 72, wherein the concentration of conductivity enhancing impurity in the first region is greater than or equal to 1 x $10^{18}cm^{-3}$.

77. (New): The method of claim 72, wherein the concentration of conductivity enhancing impurity in the first region is greater than or equal to about 1 x $10^{18}cm^{-3}$, with the second region having a impurity concentration of less than 1 x $10^{18}cm^{-3}$.